New Jersey Semi-Conductor Products, Inc.

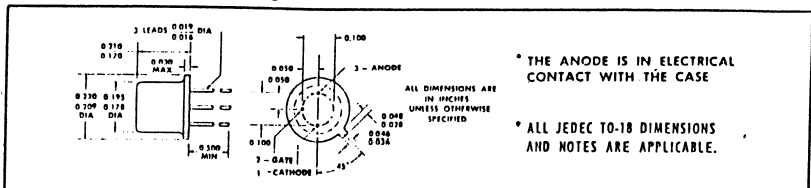
20 STERN AVE.
SPRINGFIELD, NEW JERSEY 07081
U.S.A.

TELEPHONE: (973) 376-2922
(212) 227-6005
FAX: (973) 376-8960

2N3002
SILICON CONTROLLED SWITCH

mechanical data

The devices are in a hermetically sealed welded case with a glass-to-metal seal between case and leads. Approximate weight is 0.35 grams.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		UNIT
*Continuous Forward Blocking Voltage, V_{FB} (See Note 1)	60	v
*Continuous Reverse Blocking Voltage, V_R	60	v
*Peak Forward Blocking Voltage (See Note 1)	60	v
*Peak Reverse Blocking Voltage	60	v
Peak Gate Reverse Voltage	8	v
*Continuous Anode Forward Current at (or below) 55°C Free-Air Temperature (See Note 2)	350	ma
*Continuous Anode Forward Current at 130°C Free-Air Temperature (See Note 2)	75	ma
*Average Anode Forward Current (180° Conduction Angle) at (or below) 55°C Free-Air Temperature (See Note 2)	250	ma
*Anode Surge Current (See Note 3)	6	a
*Peak Gate Forward Current (Pulse width $\leq$ 8 msec)	250	ma
*Average Gate Power Dissipation	100	mw
*Operating Free-Air Temperature Range	−65 to +150	°C
*Storage Temperature Range	−65 to +200	°C

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_F	Anode Forward Blocking Current†	V_{AK} = Rated V_{FB}, R_{GK} = 1 kΩ			20	na
		V_{AK} = Rated V_{FB}, R_{GK} = 1 kΩ, T_A = 150°C			20	μa
I_R	Anode Reverse Blocking Current†	V_{KA} = Rated V_R, R_{GK} = ∞			0.1	μa
		V_{KA} = Rated V_R, R_{GK} = ∞, T_A = 150°C			100	μa
I_{GR}	Gate Reverse Current	V_{KG} = 5 v, R_L = ∞			0.1	μa
$I_{GT(on)}$	Gate Trigger Current†	V_{AA} = 5 v, R_L = 12 Ω		5.0	20	μa
$V_{GT(on)}$	Gate Trigger Voltage†	V_{AA} = 5 v, R_L = 12 Ω, T_A = −65°C			0.9	v
		V_{AA} = 5 v, R_L = 12 Ω		0.55	0.7	v
		V_{AA} = 5 v, R_L = 12 Ω, T_A = 150°C	0.2			v
I_H	Holding Current	R_{GK} = 1k Ω		1.2	3.0	ma
		R_{GK} = 1k Ω, T_A = −65°C			4.0	ma
V_F	Peak Instantaneous Fwd. Voltage	I_F = 350 ma, (See Note 4)			1.1	v
dV/dt	Critical Rate of Anode Voltage Rise	V_{KG} = 1.0 v		400		v/μsec

NOTES: 1. This value applies when the Gate-Cathode Resistance, $R_{GK} \leq$ 1 kΩ

2. For operation above 55°C free-air temperature, refer to Anode Forward Current Derating Curve, Figure 1.

3. This rating applies for one half-cycle sine wave, 60 cps, when the device is conducting maximum rated current immediately before and after the surge. Surge may be repeated after the device has returned to original thermal equilibrium conditions.

*Indicates JEDEC registered data.

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	--- ---	0.025 15	μAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0.5 Vdc)	I_{CEX}	---	.050	μAdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0.5 Vdc)	I_{BL}	---	.050	μAdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	60	---	Vdc
Collector-Emitter Breakdown Voltage [1] (I_C = 10 mAdc, pulsed, I_B = 0)	BV_{CEO}	20	---	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	---	Vdc
Collector Saturation Voltage [1] (I_C = 150 mAdc, I_B = 15 mAdc)	V_{CE} (sat)	---	0.5	Vdc
Base-Emitter Saturation Voltage [1] (I_C = 150 mAdc, I_B = 15 mAdc)	V_{BE} (sat)	---	1.3	Vdc
DC Forward Current Transfer Ratio (I_C = 150 mAdc, V_{CE} = 10 Vdc)	h_{FE}	100	300	---
Common-Base Open Circuit Output Capacitance (V_{CB} = 10 V, I_E = 0, f = 100 kHz)	C_{ob}	---	8.0	pF
Delay Time (V_{CC} = 30 V, I_{CS} = 150 mA, I_{B1} = 15 mA)	t_d	---	20	ns
Rise Time (V_{CC} = 30 V, I_{CS} = 150 mA, I_{B1} = 15 mA)	t_r	---	75	ns
Storage Time (V_{CC} = 6 V, I_{CS} = 150 mA, I_{B1} = 15 mA, I_{B2} = 15 mA)	t_s	---	300	ns
Fall Time (V_{CC} = 6 V, I_{CS} = 150 mA, I_{B1} = 15 mA, I_{B2} = 15 mA)	t_f	---	200	ns
Current Gain-Bandwidth Product (I_C = 20 mA, V_{CE} = 20 V, f = 100 MHz)	f_T	250	---	MHz

[1] PULSE TEST: Pulse width ≤ 300 μs, duty cycle ≤ 2%

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